VCSEL and Smart Pixel Research for VLSI Photonic Systems

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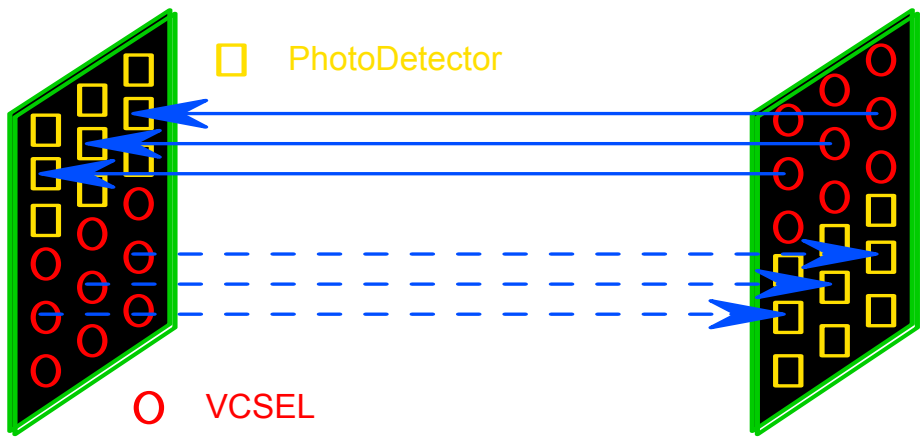
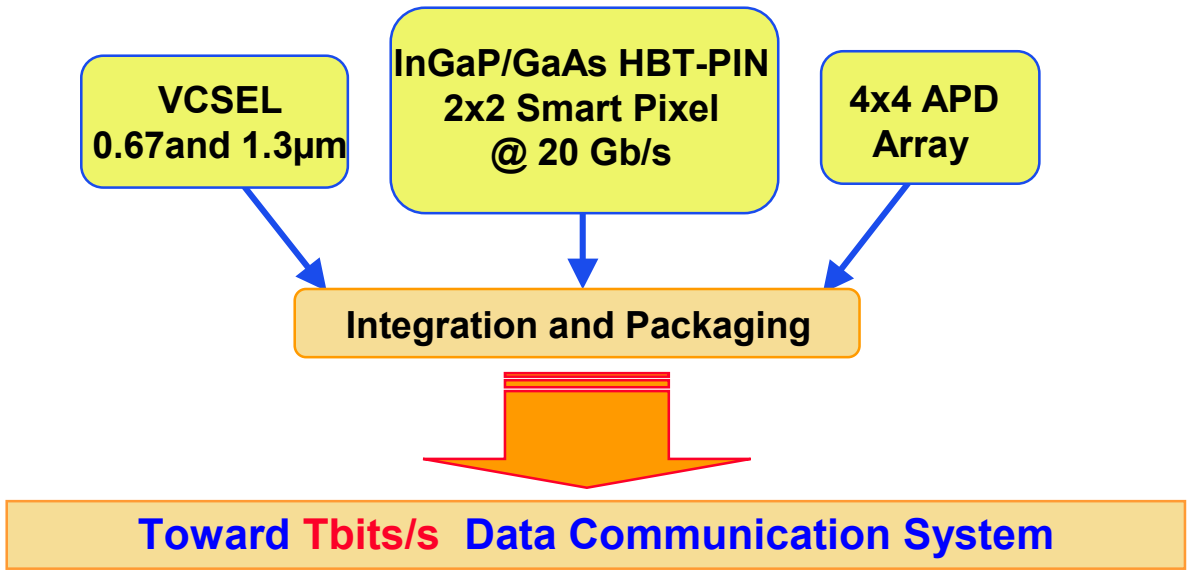
VCSEL and Smart Pixel Research
Objective

Development of *III-V compound semiconductor-based* VLSI Photonic System employing low-power VCSEL and smart pixel arrays for use in a high-speed data communication system



VCSEL and Smart Pixel Research - ***Approach***



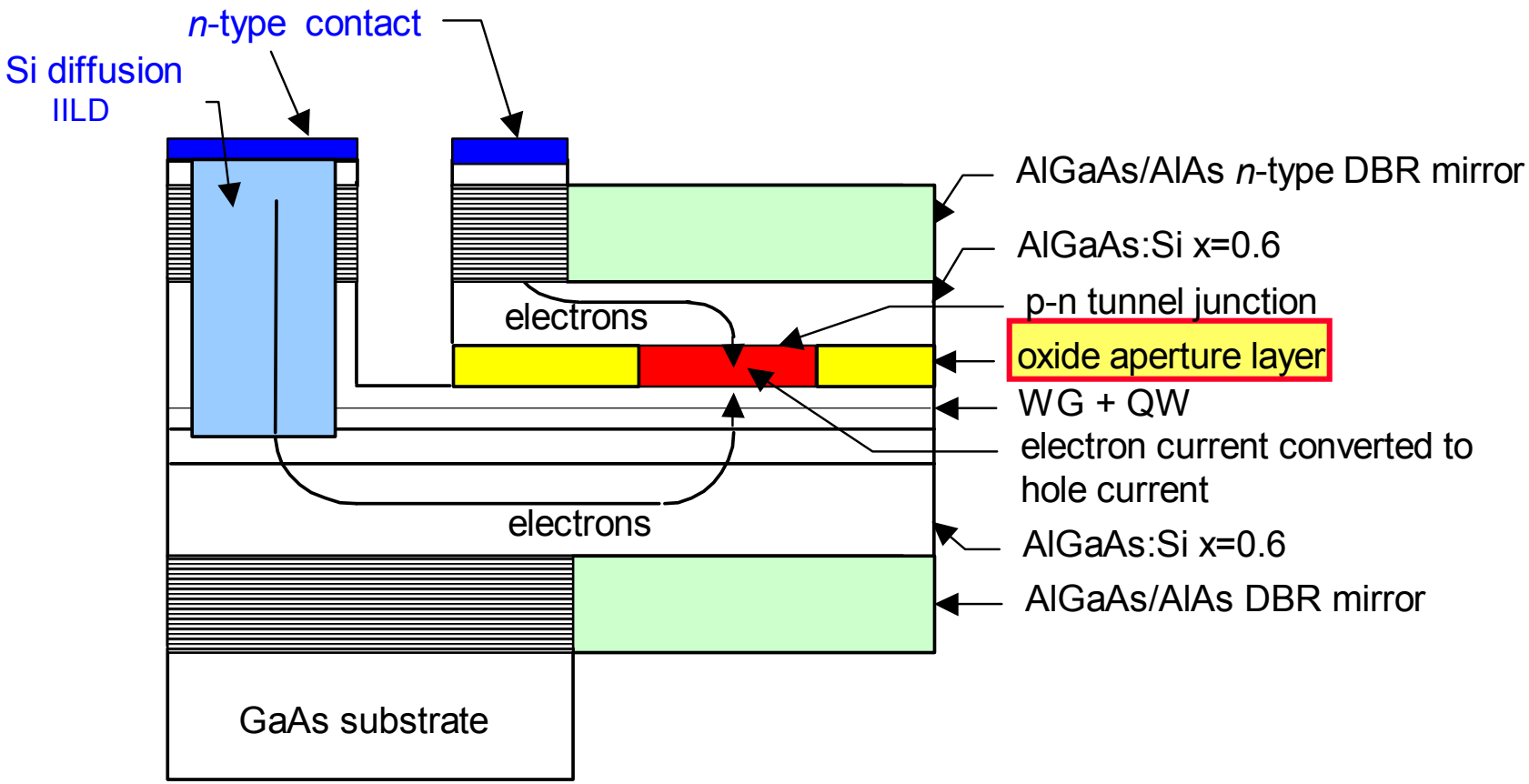
- Task 1 - Low power VCSEL 670 nm and 1330nm
- Task II - Smart Pixel Development
  *2x2 HBT/PIN Smart Pixel Array at 20 GB/s
- Task III - Package, Assembly and Characterization of Smart Pixel Arrays
- Task IV - High speed avalanche photodiode 4x4 array

670 nm InAlGaP Native-Oxide VCSEL Development

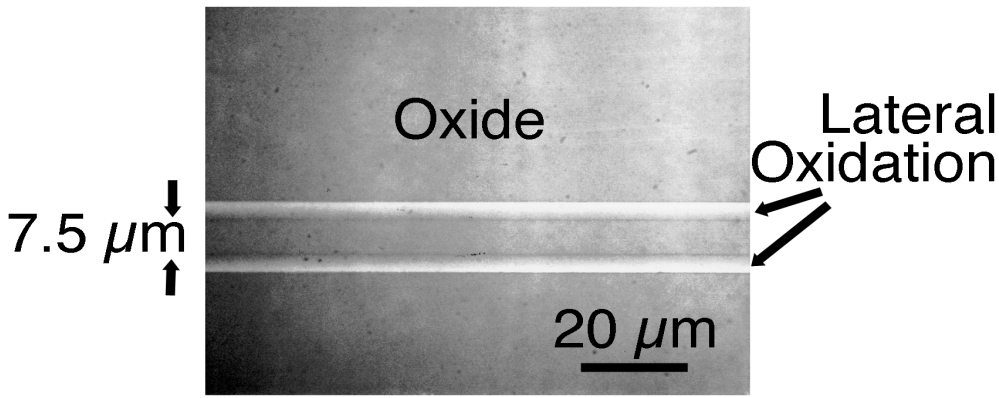
- Advantages:
  - InAlGaP injection lasers emitting in the red spectral region can be used for plastic-fiber based optoelectronic systems.
  - Integration with high-speed InGaP/GaAs HBT circuits will permit high-density, high-speed optical interconnects to be realized
- Challenge:
  - InAlGaP VCSELs demonstrated to date typically employ thick epitaxial Bragg mirrors due to the low index of refraction contrast for these materials
- Current Approaches:
  - Incorporating native-oxide DBR mirrors to achieve compact-cavity VCSELs suitable for integration with HBT-receiver circuits.
  - Using tunnel-injection confinement layers for efficient current injection into the active region of the VCSEL

Schematic Diagram of 670 nm Native-Oxide VCSEL

- Employs AlAs/GaAs oxide DBR mirror and tunnel current injection

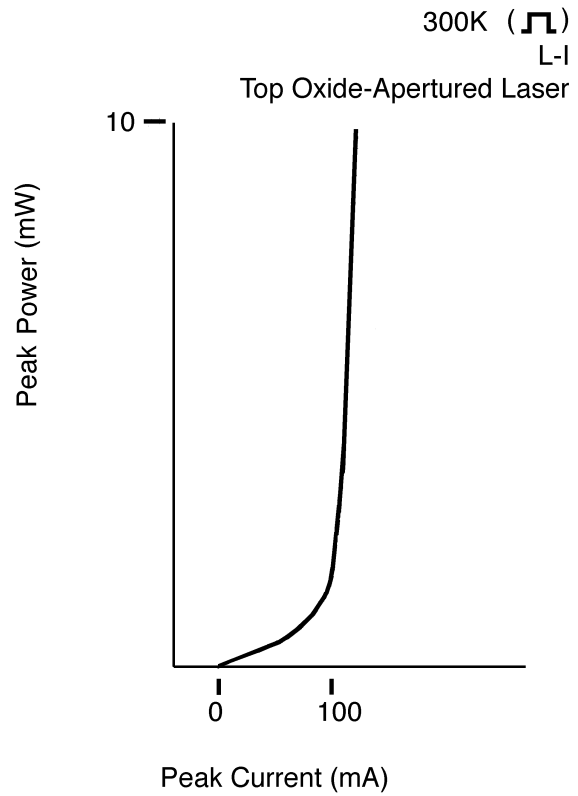


SEM Photo and L-I Curve of a Native Oxide Confined $In_{0.5}(Al_xGa_{1-x})_{0.5}P$ MQW Laser

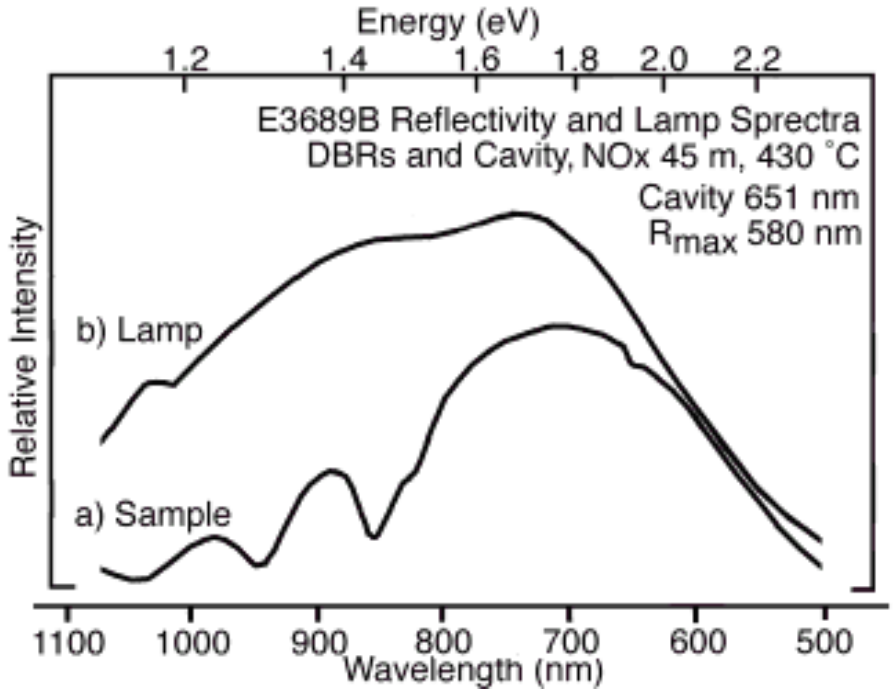


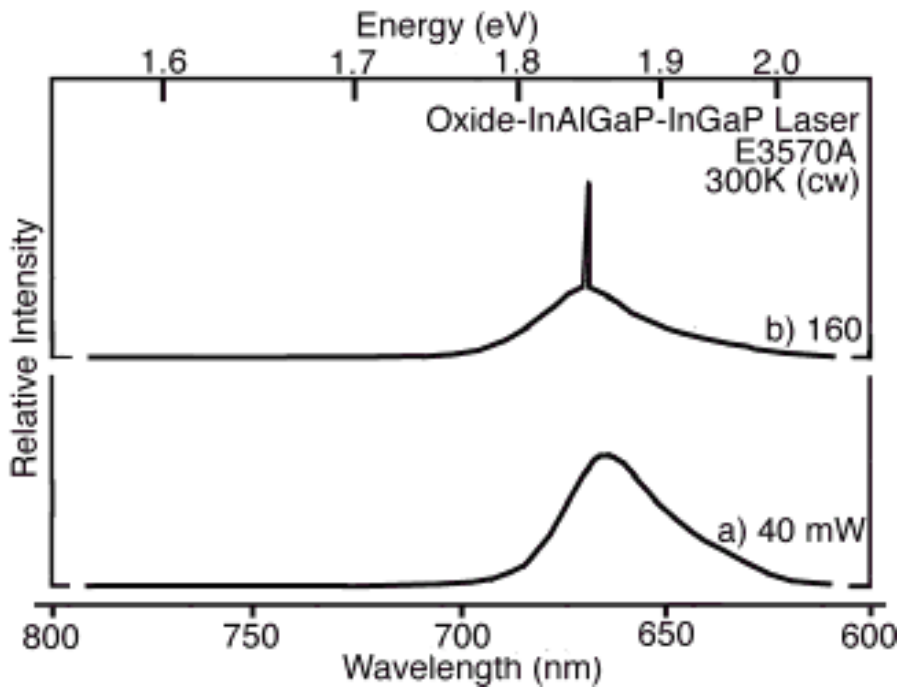
- Lateral selective oxidation of AlGaAs regions for lateral confinement performed in oxidation furnace with water vapor at ~450°C.
- Patterned into 10 μm stripes and laterally oxidized to form a 7.5 μm upper *p*-type aperture for current and optical confinement.

- Achieved electrically pulsed lasing operation at 650 nm.



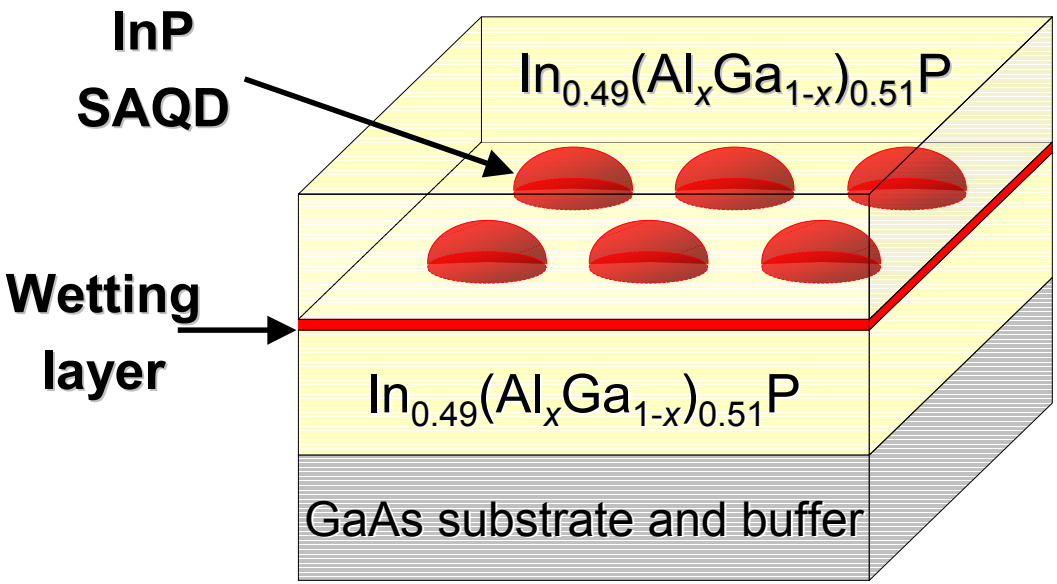
Demonstration of InAlGaP Optically Pumped Native-Oxide Confined Laser

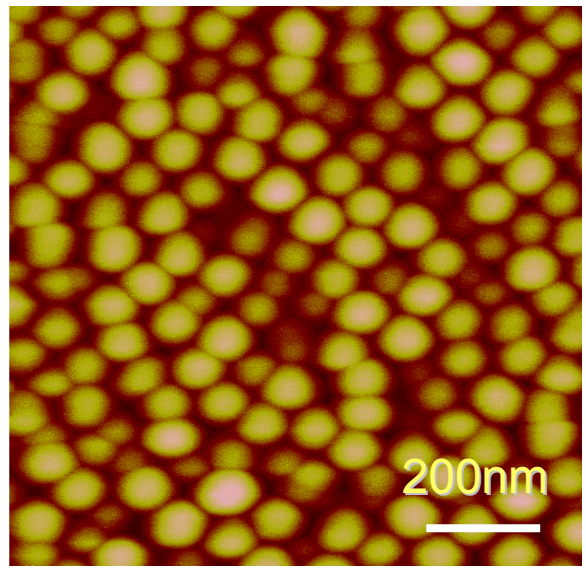




- Oxidized AlGaAs/InAlP DBR mirror spectral reflectivity for compact-cavity visible VCSEL
- Oxide-aperture InAlGaP/InGaP MQW optically pumped laser operates CW at 300K.

$InP/In_{0.49}(Al_xGa_{1-x})_{0.51}P$ Quantum Dot Heterostructure (QDH)

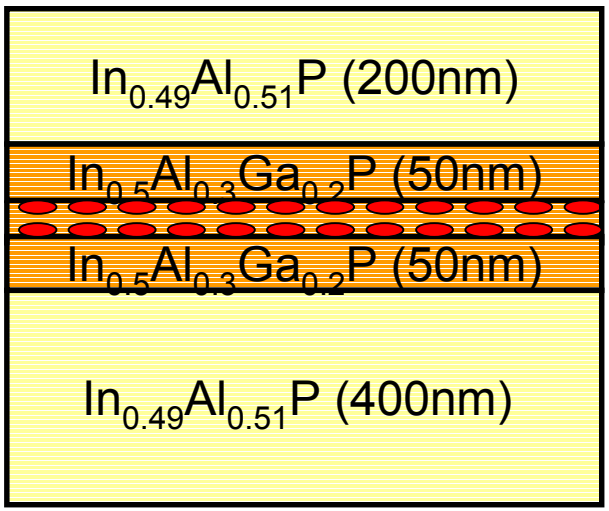




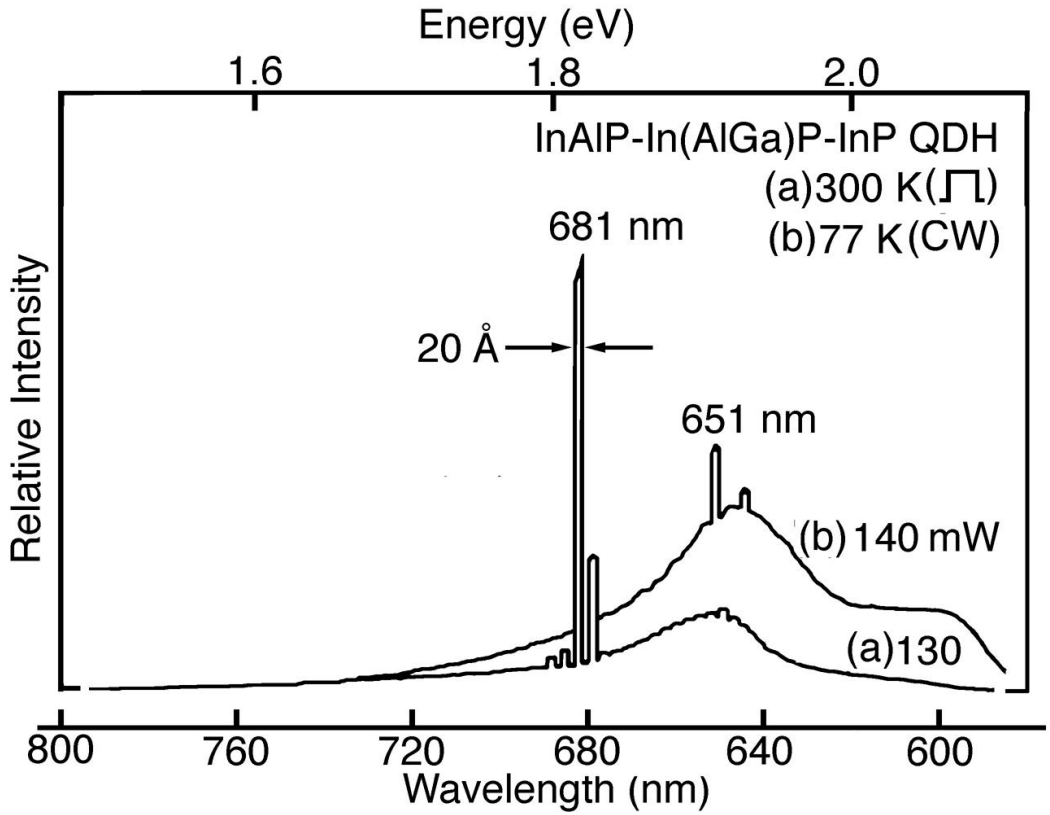
AFM image 1x1 μm

- MOCVD grown at 650ºC for 15ML
- Small and dense SAQD formation
- Dominant QD size = ~15~20nm
- QD density = ~$1.5x10^{10}cm^{-2}$

Optical Spectra of DQDH InP-QD/$In_{0.5}Al_{0.3}Ga_{0.2}P$/$In_{0.49}Al_{0.51}P$ Laser



- QD - 7.5 ML InP
- Barrier - 10 nm InAlGaP



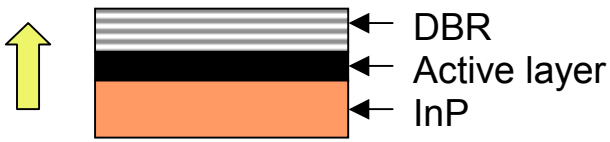
- CW lasing at 651 nm at 77K
- Pulsed lasing at 681 nm at 300K

1330 nm VCSEL Development

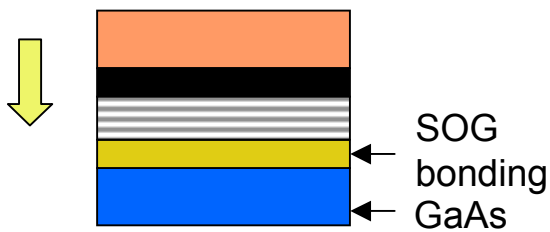
- Purpose
  - Development of InGaAs based long wavelength VCSELs with highly stable operation properties
- Challenge:
  - Lack of efficient distributed Bragg Reflection (DBR) mirrors
  - Unstable emission mode
- Current Approaches:
  - Development of ex-cavity wafer bonding process for VCSEL fabrication
  - Development of high refractive index difference materials such as GaAs/Al-oxide, Si/SiO_2 and Si/AlO_x for DBR mirror applications on InP
  - Utilizing thermal and polarization stable quantum wires in the active region of the laser

Process Flow for 1330 nm VCSELs

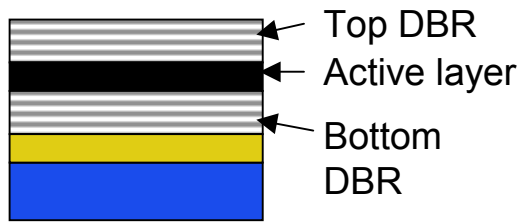
1. Epitaxy and bottom DBR deposition



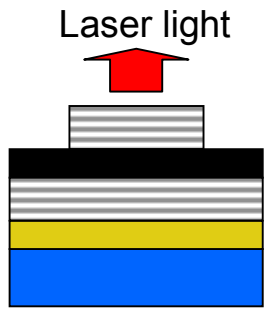
2. Wafer bonding using spin-on-glass (SOG) or metals



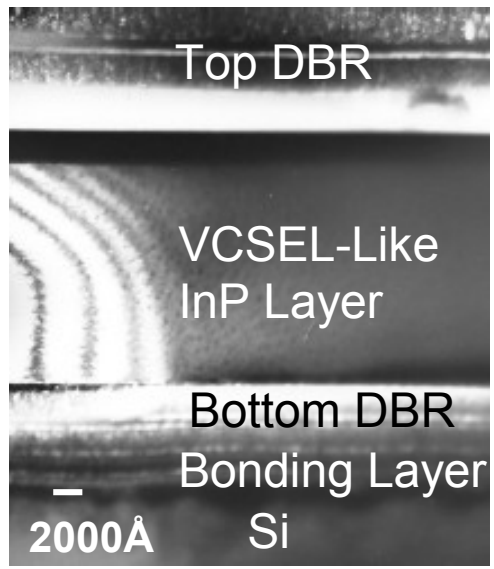
3. InP substrate removal and top DBR deposition



4. Device patterning

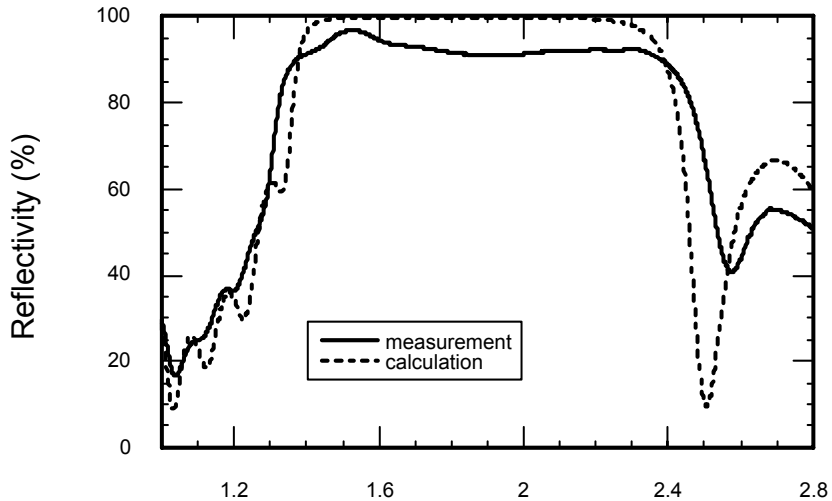


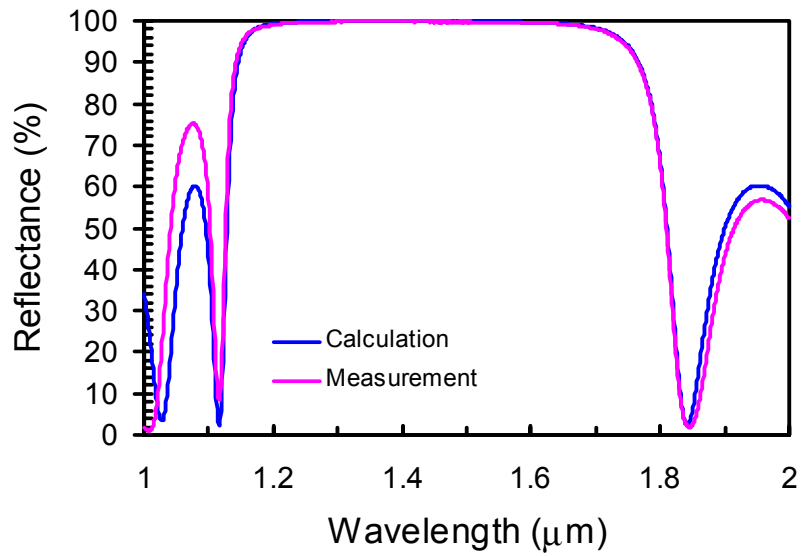
VCSEL Structure By Wafer Bonding

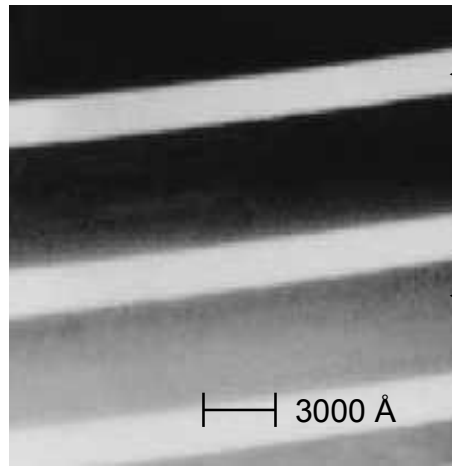


- High efficiency oxide DBR mirror deposited on InP wafer
- Bonding the VCSEL-like InP/DBR structure to Si substrate
- Top DBR mirror deposited on InP/DBR/Si structure

Characteristics of GaAs/Al-oxide and AlO_x/Si DBRs on InP

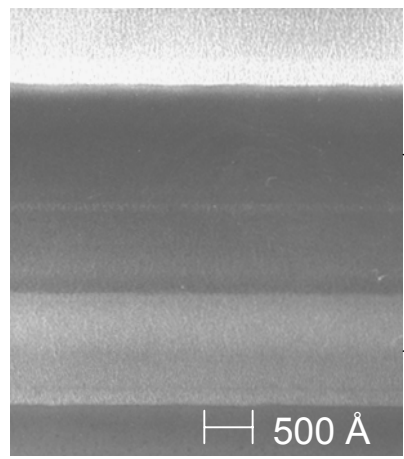






Poly-GaAs (1200 Å)

VLT-MBE grown and wet oxidized Al-oxide (3200 Å)

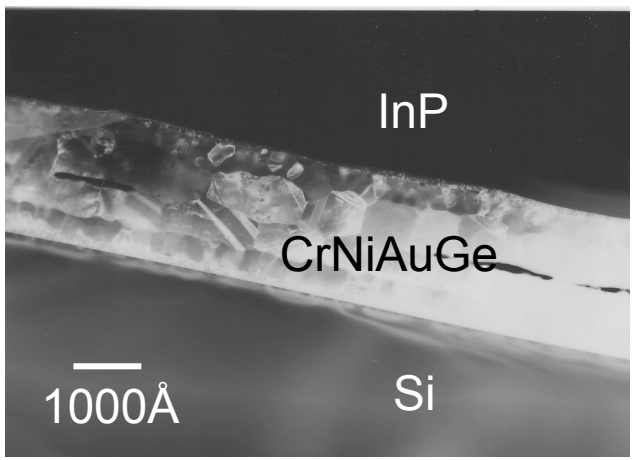


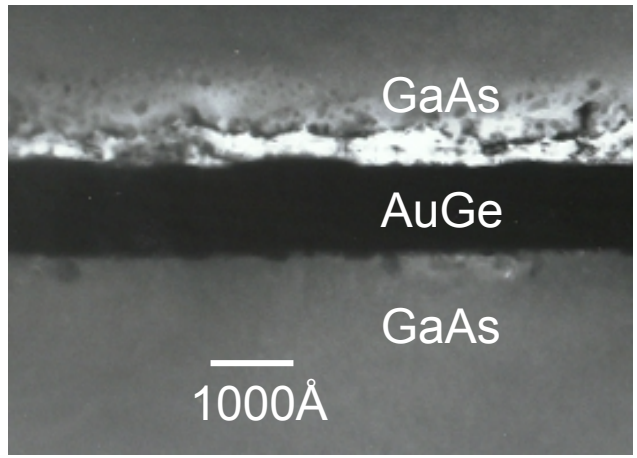
E-beam evaporated Al-oxide (2350 Å)

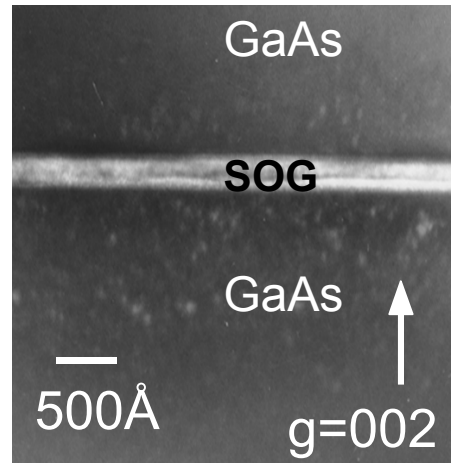
Si (950 Å)

TEM picture

DBR Mirror Bonding Results





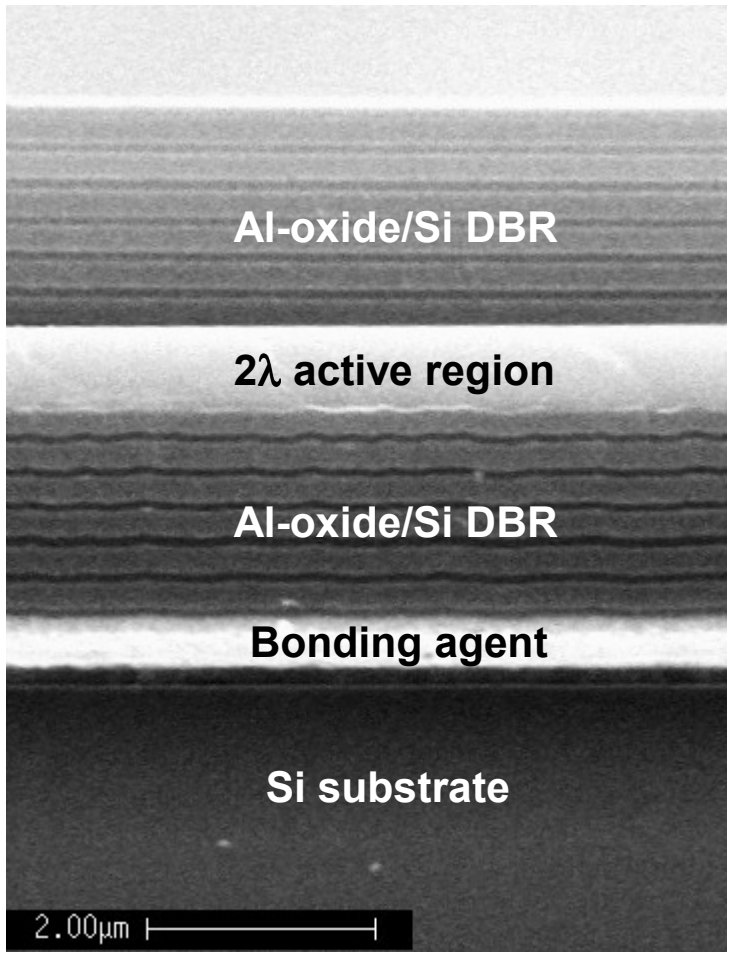


Metalllic Bonding

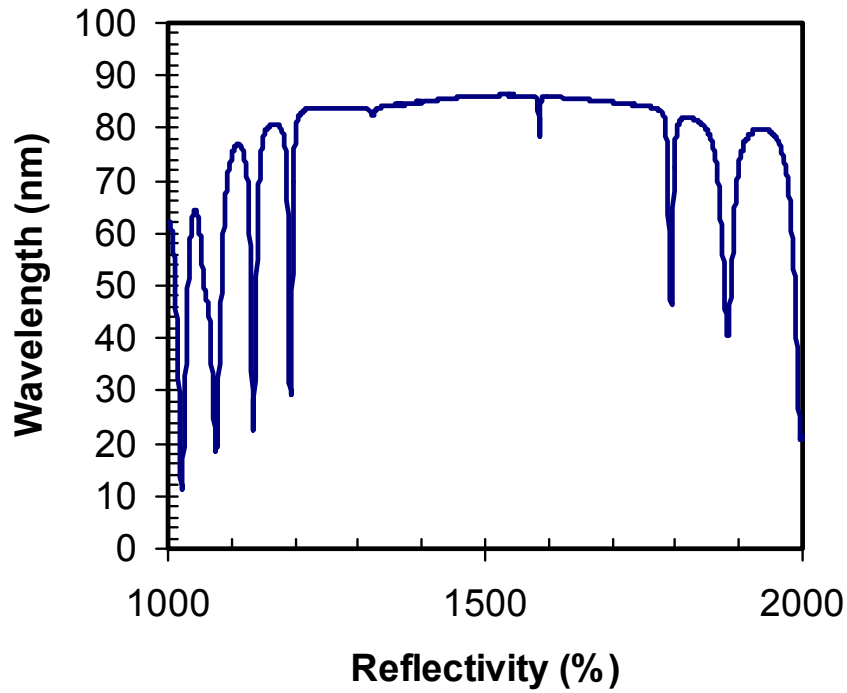
Spin-on-glass (SOG) Bonding

- Demonstrated wafer bonding of GaAs/InP, Si/InP for long-wavelength VCSEL fabrication process
- Bonding temperature as low as ~ 420ºC

Completed 1.55 μm VCSEL by Wafer Bonding

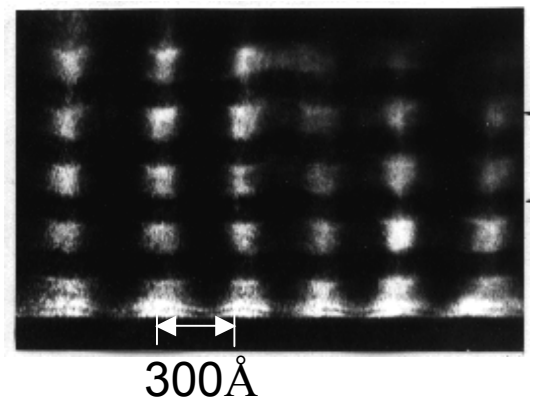


- Completed VCSEL cavity bonded to Si substrate consists of 6-period top and bottom Al-oxide/Si DBRs and an InGaAsP active region.

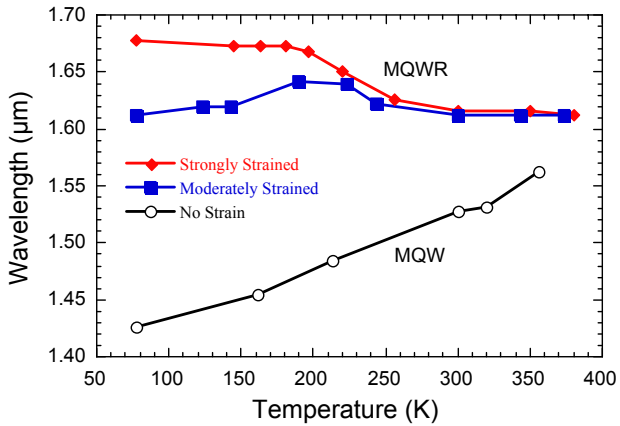


Highly Stable Quantum Wire Material for 1.55 μm VCSEL Applications

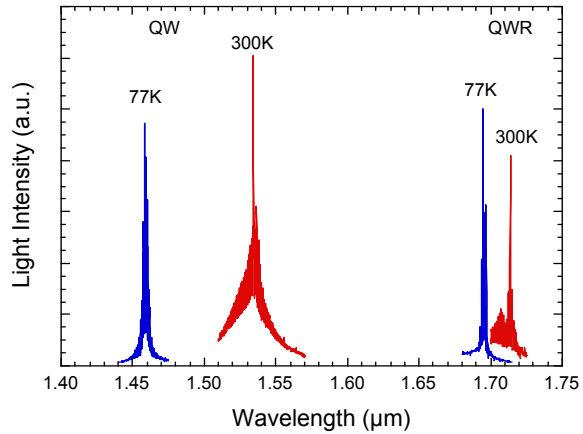
XTEM micrograph of InGaAs QWRs



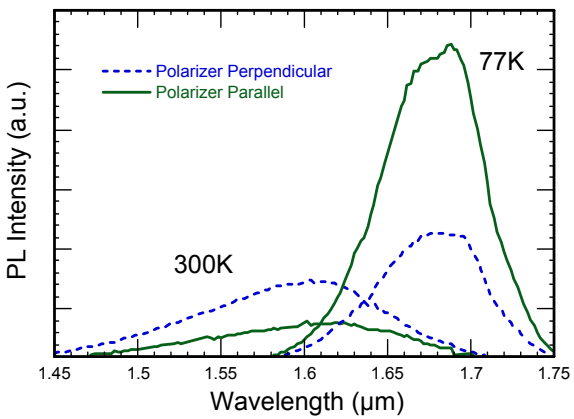
Temperature stable QWR emission



Temperature stable lasing wavelength (1Å/C) in QWR laser



Anisotropic polarization in surface photoluminescence



- Temperature induced gain and DBR mirrors mismatch can be eliminated
- Stable polarization in surface emission
- Suitable for high speed and high power 1.55 μm VCSEL applications

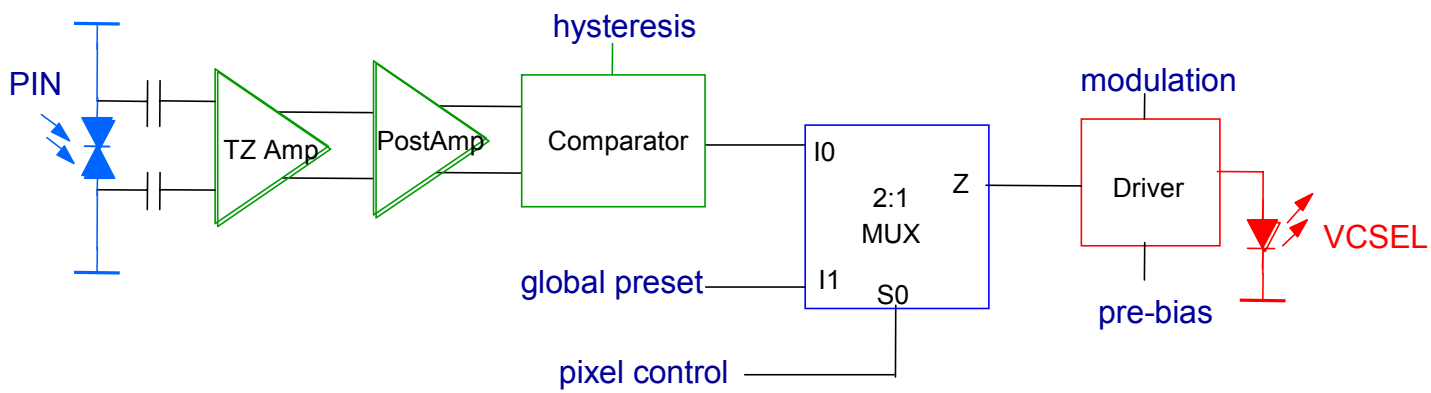
University of Illinois at Urbana Champaign
Princeton University
University of Texas at Austin

Progress and Future Milestones of VCSEL Development Task

- Low-threshold 670 nm InAlGaP injection lasers:
  - Demonstrated Al-oxide/InAlP DBR mirrors and native-oxide defined visible laser operates CW at 300K
  - Demonstrated novel InP quantum dot laser emitting at 680 nm.
- 1.3-1.6 μm InGaAs VCSELs:
  - Developed high-reflectance (>99.9%) DBR mirrors on InP using VLT-MBE grown and water vapor oxidized GaAs/Al-oxide and Si/AlO_2 over a wide spectral range
  - Developed a robust wafer bonding process for VCSEL fabrication
  - Discovered thermal and polarization stable photoluminescence in InGaAs quantum wire heterostructures above 200K suitable for VCSEL applications
- Future Work
  - Incorporate tunnel-injection confinement layers to achieve 670 nm compact-cavity VCSEL suitable for integration with HBT-receivers
  - Process integration for 1.3-1.6 μm quantum wire VCSELs

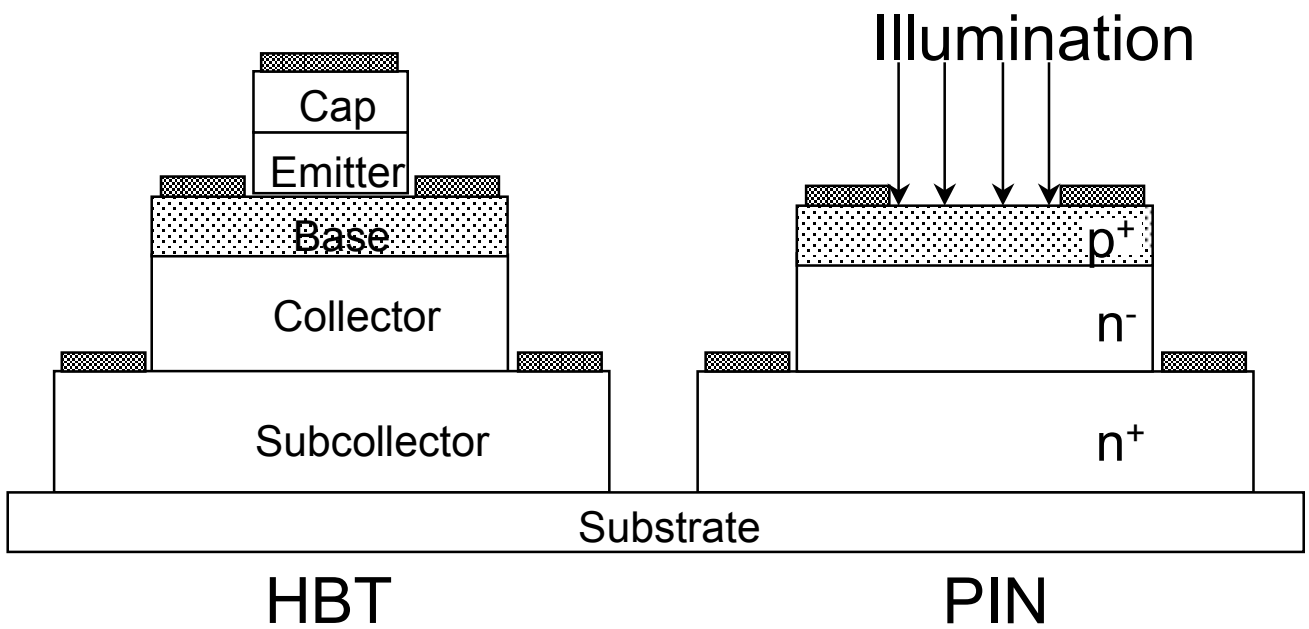
Task II: Smart Pixel Array Development

- **Program Goal:**
  20 Gb/s smart pixel, 2 x 2 array (Total capacity ~ 80 Gb/s)
- **UIUC InGaP/GaAs HBT and PIN Technologies**
  - Baseline HBT performance: f_T = 65 GHz, f_{max} = 110 GHz
  - On-Wafer PIN Photodetector
  - Low Power Design, < 100mW per Channel
  - AC Coupled Front-End Analog Receiver
  - Digital Logic Circuit
  - Optical Output Using Low Power VCSEL

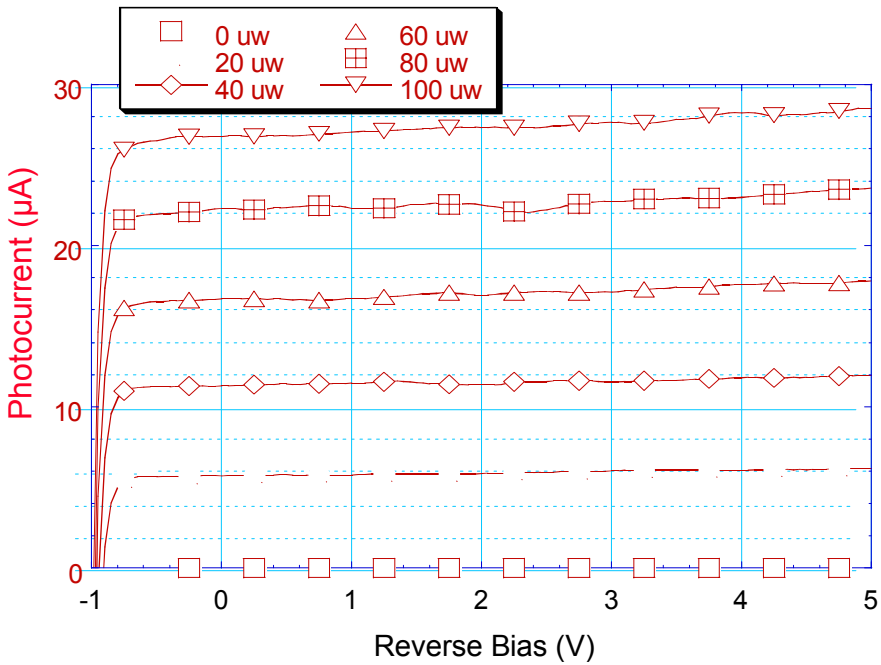


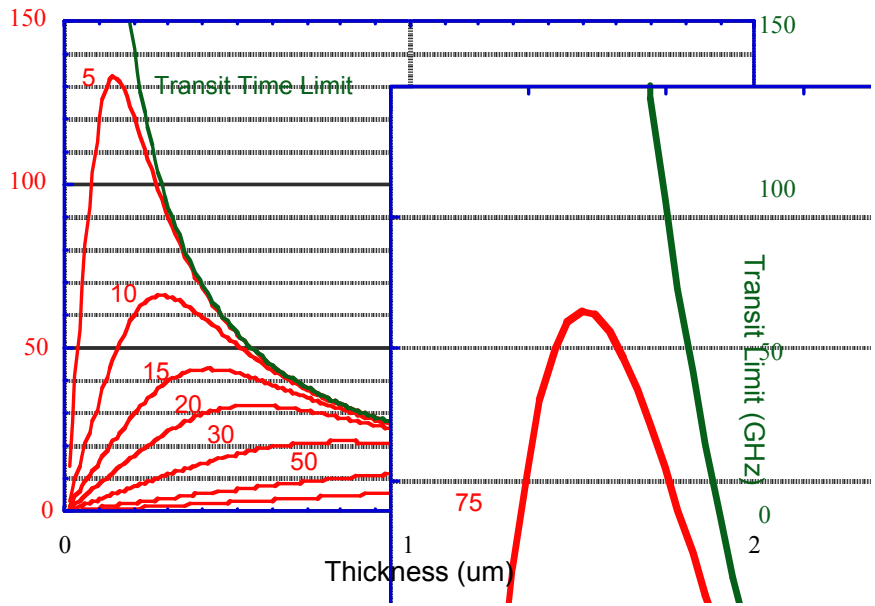
Basic InGaP/GaAs HBT/PIN Structure

- PIN and HBT devices incorporated into a single heterostructure
- Carbon doping used in the base for high reliability
- 4- inch MOCVD growth capability
- Standard structure well established at UIUC



Characteristics of High Speed PIN Photodetectors

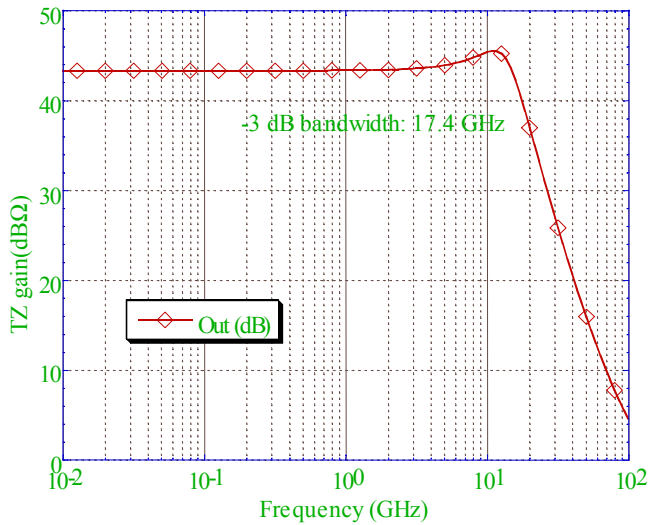


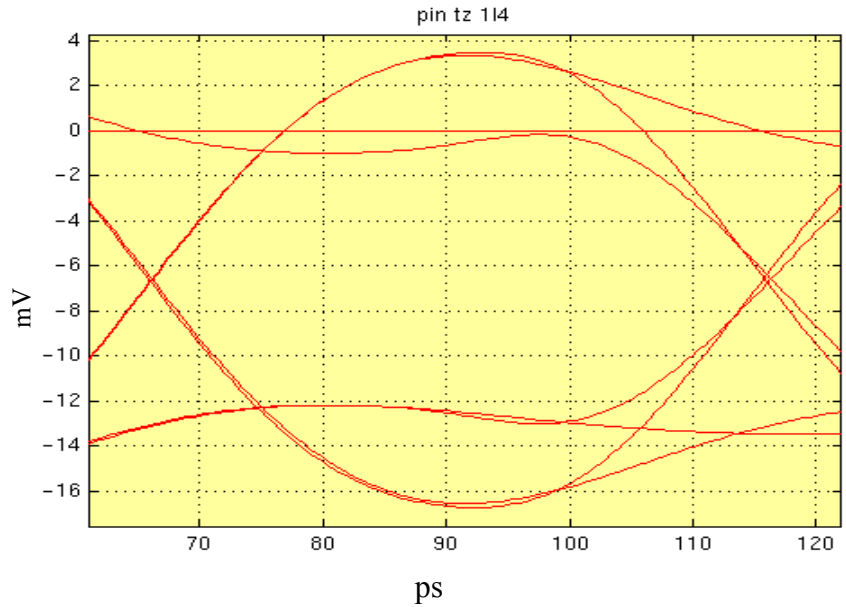


- DC Response measurement
  - For a 50-μm diameter PIN
  - Illumination: 0-100μw
  - Responsibility: 0.3A/W

- Calculated 3-dB bandwidth
  - Combining carrier transit time effect
  - Parasitic effect dominates at large area detectors (RC)

Design and Simulation of 20 Gb/s Photoreceiver Circuits

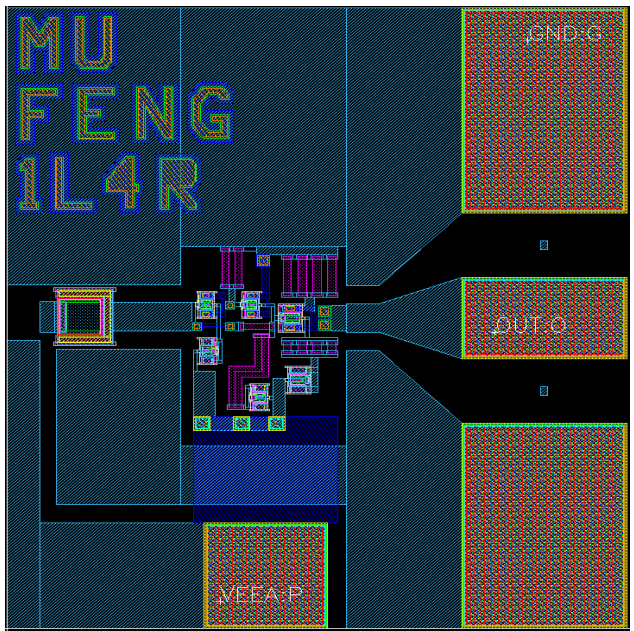




- **Simulated TZ gain of PIN_TZ_1L4**
  - PIN with diameter of 25μm
  - TZ gain 43.3 dBΩ
  - -3dB bandwidth 17.4 GHz
  - DC coupled with single-ended input and output

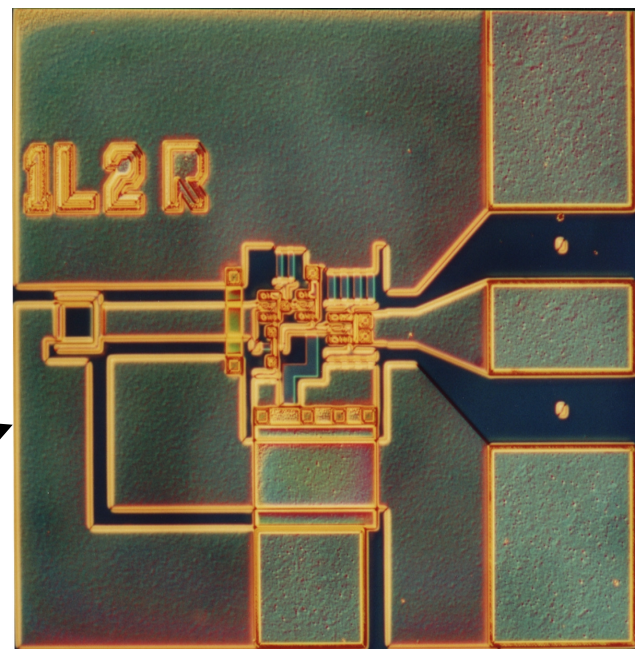
- **Simulated eye diagram of PIN_TZ_1L4 at 20Gb/s**
  - Input signal swing from 10μA to 100μA
  - 25% overshoot and undershoot
  - Sensitivity: -7.84dBm for 10^{-9} error rate at 20Gb/s
  - Eye widely opened at 20Gb/s

Single Channel 20 Gb/s Photoreceiver Circuits



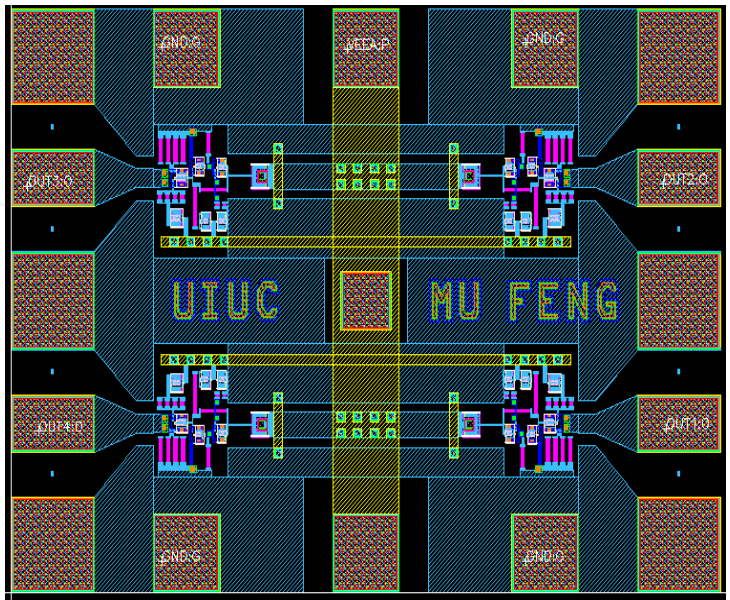
- Layout of PIN_TZ_1L4 photoreceiver circuit design.

- **Layout of PIN_TZ_1L4 single channel photoreceiver circuit**
  - Single-ended input from photodetector
  - Differential output to drive digital circuits
  - Fabricated by Alpha-Network device Inc. (NDI)
  - OEIC chip received in April, 2001



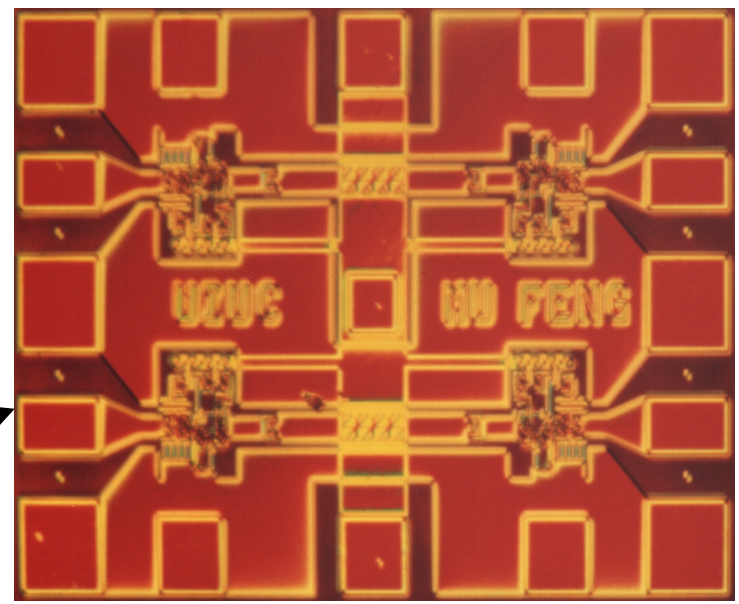
- Micro- photograph of fabricated chip PIN_TZ_1L2 with speed of 20Gb/s

20Gb/s 2×2 Photoreceiver Array



- Layout of 2x2 photoreceiver array for 80Gb/s

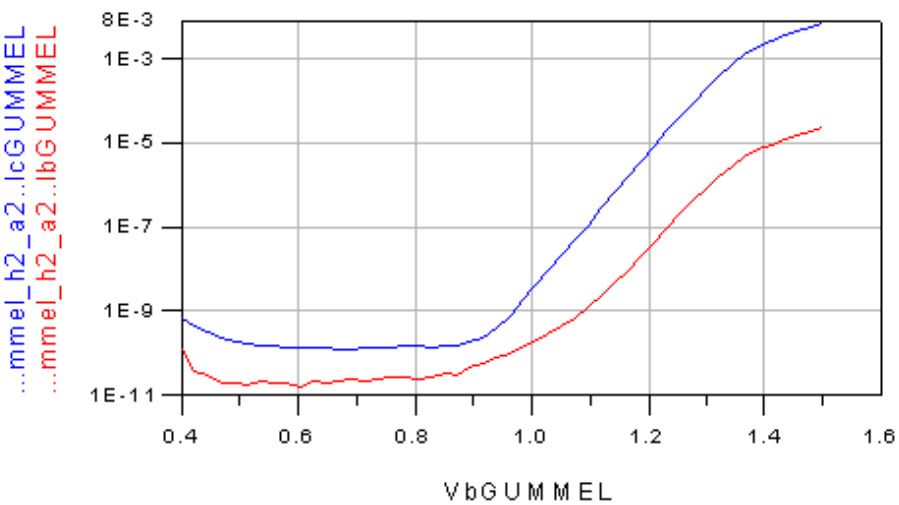
- **Layout of 2x2 photoreceiver array for 80Gb/s**
  - Power consumption: 320mW
  - DRC and LVS checked
  - 25μm diameter PIN
  - Distance between adjacent PIN: 250μm
  - 50Ω coplanar transmission line used



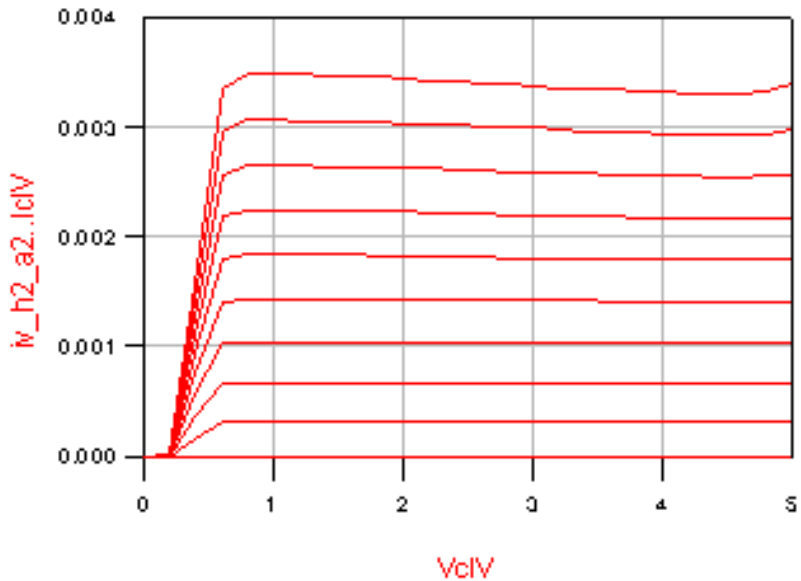
- Chip Microphotograph of 2x2 photoreceiver array aimed at the speed of 80Gb/s

Initial DC Testing Results

- Fabricated by Alpha-NDI.
- InGaP/GaAs OEIC Chips received in April, 2001
- 10 to 20Gb/s RF testing is under way



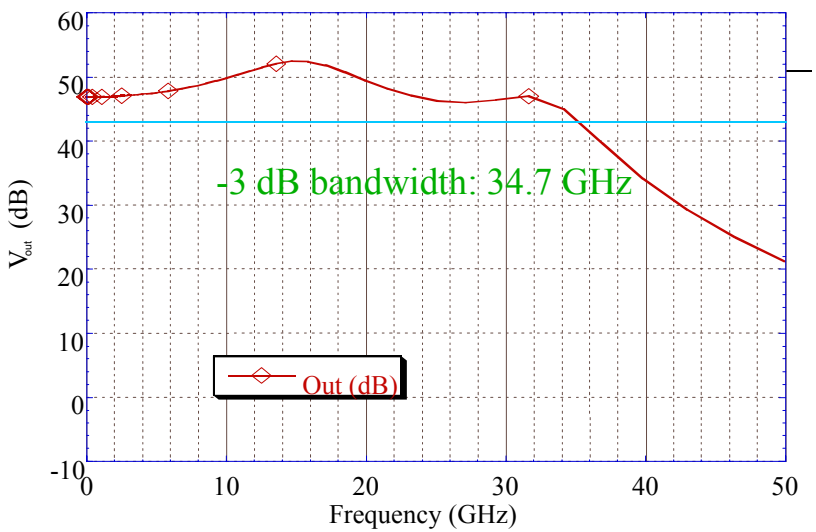
- Measured forward Gummel plot

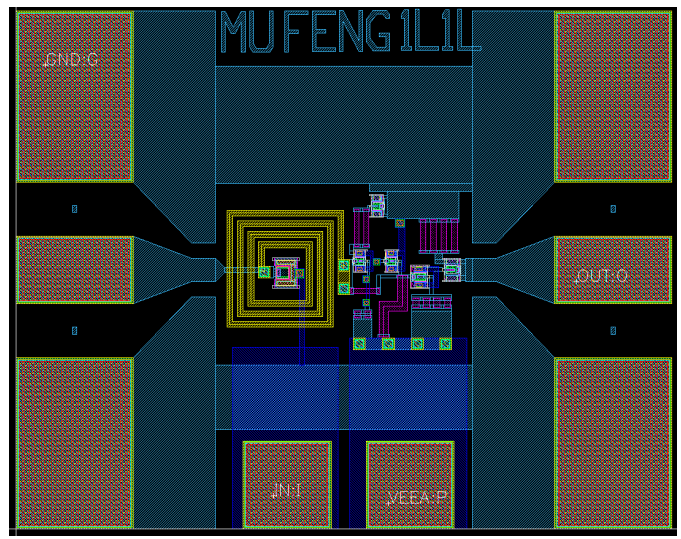


- Measured I-V curve for HBT H2

40 Gb/s Photoreceiver Design Using Inductor Peaking Technique

- **10-μm diameter PIN integrated with TZ_1L1_L (–3dB bandwidth is 8.2GHz)**
- **–3dB bandwidth increases to 34.7GHz due to the effect of added 1.5nH inductor**
- **Photodetector is placed inside inductor to avoid illumination on transistors**
- **Chip can be tested with both electrical and optical input**
- **Note: introduce peaking into the frequency response**





- Simulated TZ gain of PIN_TZ_1L1_L for 40Gb/s
- Layout of PIN_TZ_1L1_L for 40Gb/s

Progress and Future Milestones of Smart Pixel Array Task

Progress:

- Designed and simulated 10, 20 and 40Gb/s photoreceivers
- Designed 2-dimension (2×2) photoreceiver arrays as fast as 80Gb/s
- Designed 10Gb/s TIA using IBM SiGe technology
- Photoreceiver circuits fabrication completed by NDI and chips received in April, 2001

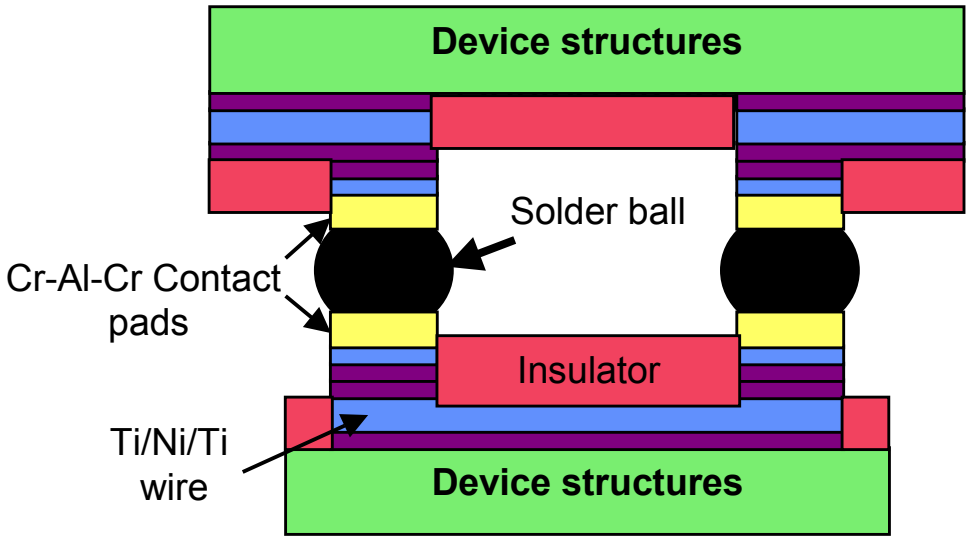
Future Milestones:

- 10Gb/s and 20Gb/s RF/Optical Testing
  - DC Measurement (I-V, Gummel Poon, temperature dependent)
  - RF Measurement (S-parameter)
  - Eye diagram, noise, and sensitivity measurements
- 40Gb/s photoreceivers Design
  - Using IBM BiCMOS7HP
  - Need to define reasonable noise, size, power, and loading requirements for 40 Gb/s operation as well as target performance specifications

Task III: Heterogeneous Material Integration

- Develop heterogeneous materials integration using direct wafer fusion and bump-bonding techniques for packaging and assembly of components for board-to-board data communications
- Materials to be bonded are GaAs, InP and Si
- Design of 2x2 and 8x8 ball grid arrays and processing optimization in wafer bonding for electrical performance
- Approach
  - Design and formation of Indium-based solder ball grid array
  - Interconnect patterning on planarized mesa

Flip-chip Bump Bonding Technology: Solder Requirements

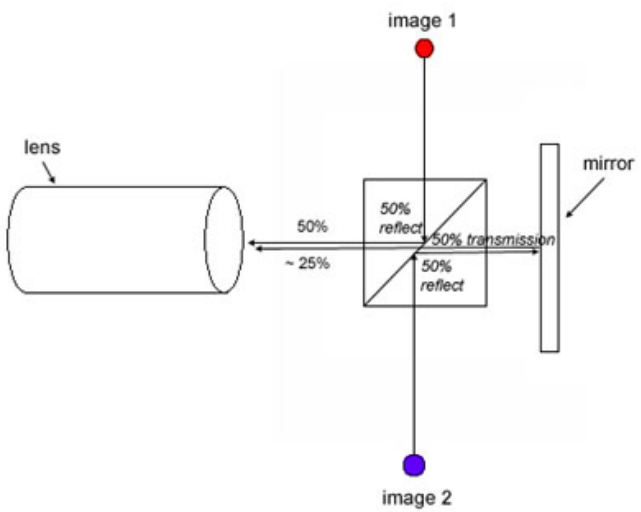


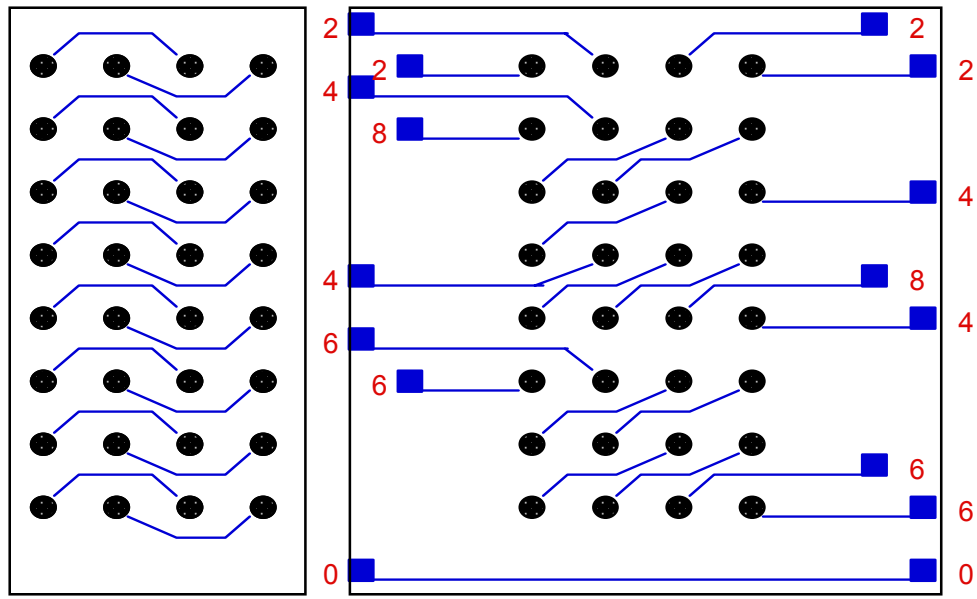
Cross-Section of Solder Contact Design

- Low melting temperature (< 400 °C)
- High conductivity
- High process yield
- Low cost
- Environmental Friendliness: Avoid toxic metals (Cd, Pb..)
- Self-alignment: De-wetting/Surface Tension abilities

Flip-chip Bump Bonding Technology Using Indium-Based Solder Balls

Bonding samples through arrays of 4x8 solder balls

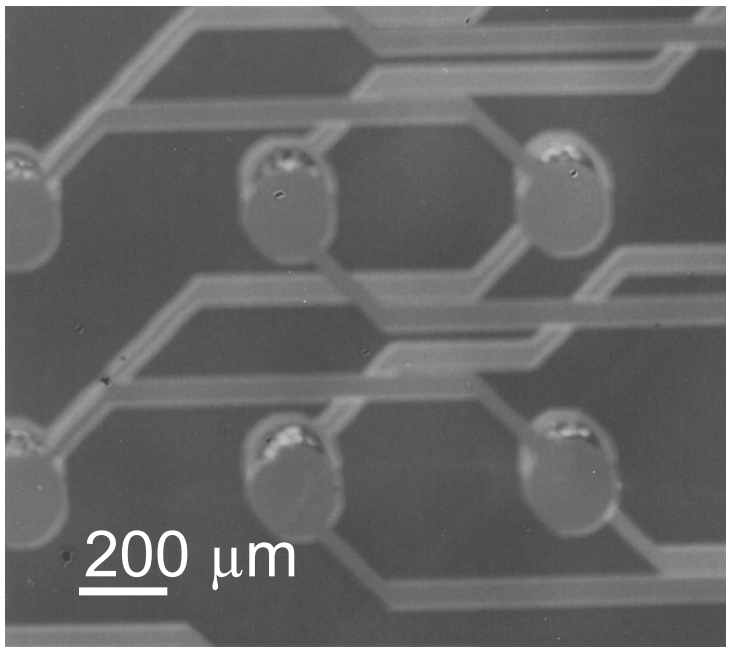


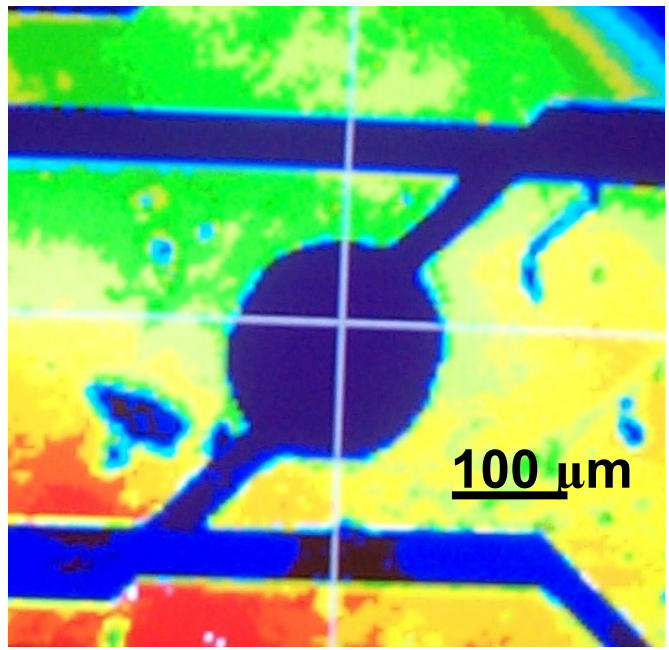


Top sample Bottom sample

- Indium-based solder balls (Ø = 50μm) patterned glass slides were used
- Demonstrates bonding capability in 4x8 array of indium-based solder balls
- Good conductance through bonds
  - Conductance was measured through 2, 4, 6, and 8 bonds in series

Optical and Infrared Micrographs of Flip-chip In-Sn Solder Bump Bonded Structures

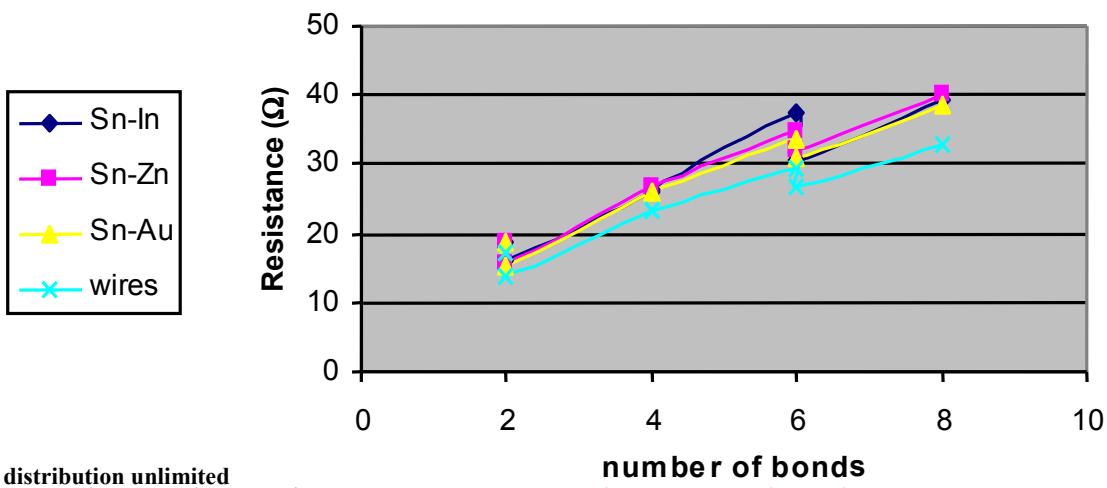




- Successfully bonded the entire array of 4x8 In bumps on two wafers ≤ 200ºC using 150μm diameter indium solder balls
- Bonding using 50 μm diameter In solder balls also demonstrated.

Flip-chip Bump Bonding Results Using Various Indium-Based Solder Balls

Solder Material	In-Sn (52%:48%)	Zn:Sn (28%:72%)	Au:Sn (40%:60%)
Melting Temperature	117 °C	325 °C	310 °C
Bonding Temperature	<200° C	~400° C	~400° C
Resistivity	9.68E-8 Ω-m	9.94E-8 Ω-m	7.88E-8 Ω-m
Process Difficulty	Easy	Difficult	Difficult

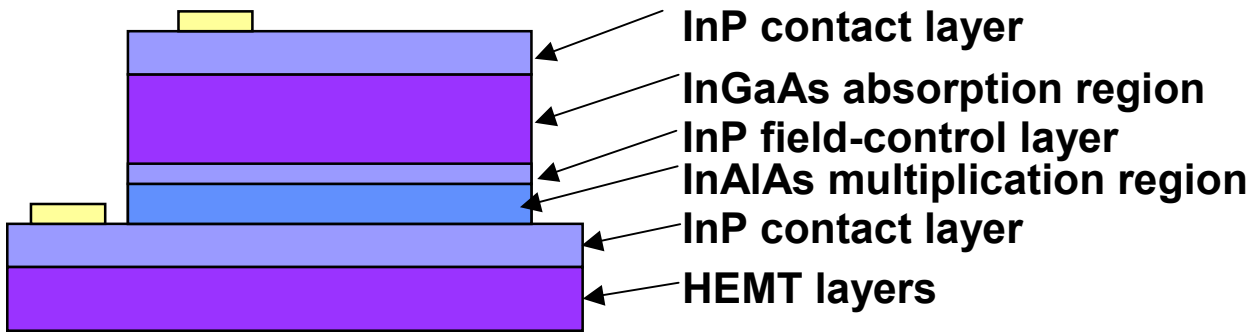


Progress and Future Milestones of Heterogeneous Material Integration Task

- Indium-Based Flip-Chip Bump Bonding:
  - Successfully bonded the entire array of 4x8 In bumps on two glass slides below 200ºC using 50μm diameter In-Sn solder balls
  - Highly reproducible process developed
  - Indium bonds show no noticeable added resistance (<9E-8 Ω-m)
- Future Work:
  - Lower electrical resistance further using Au coated Indium bumps
  - Integrate smart pixels by bonding

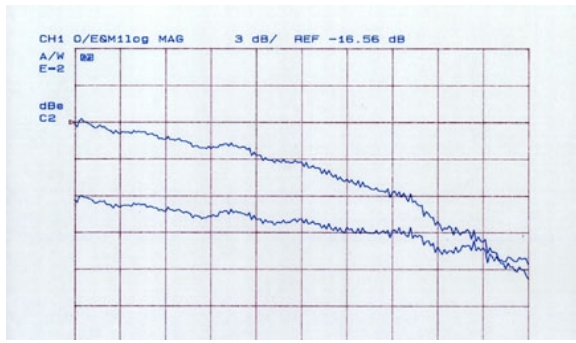
Task IV: Avalanche Photodiode (APD) Array Development

- Objective: Develop high bandwidth, high sensitivity AlInAs/InGaAs APD arrays for application at both short and long communication wavelength
  - Demonstrate high bandwidth, high sensitivity AlInAs/InGaAs APDs
  - Integrated into 2x2 and 4x4 arrays with HEMT receivers with bandwidths of 2.5 - 5 GHz.
  - Transfer technologies to industrial partners



High Bandwidth Integrated APD and HEMT Receiver Circuits

0 GHz 20GHz



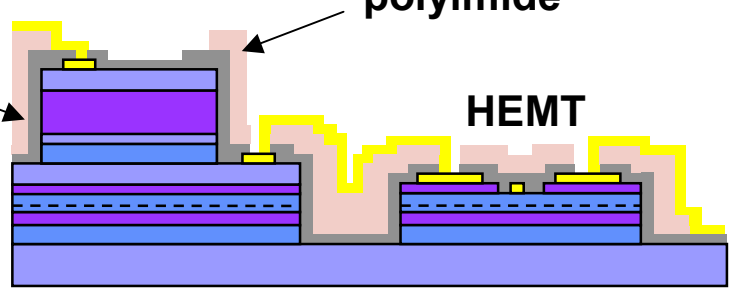
0 GHz 20GHz

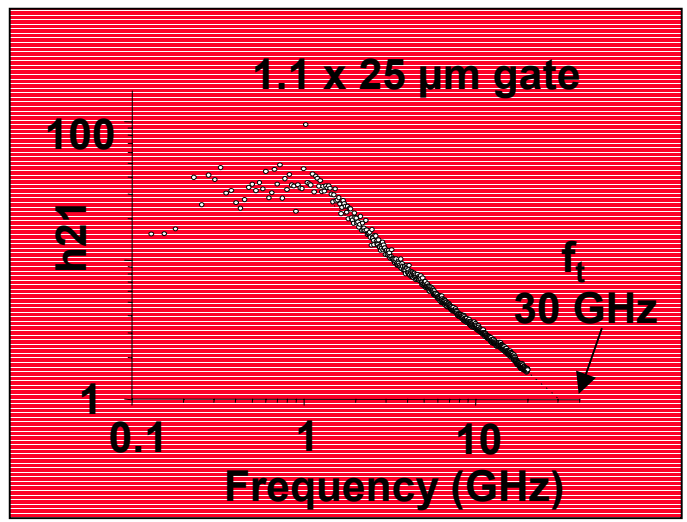
Φ=20μm APD

Bandwidth	Gain
13GHz	1
9 GHz	3

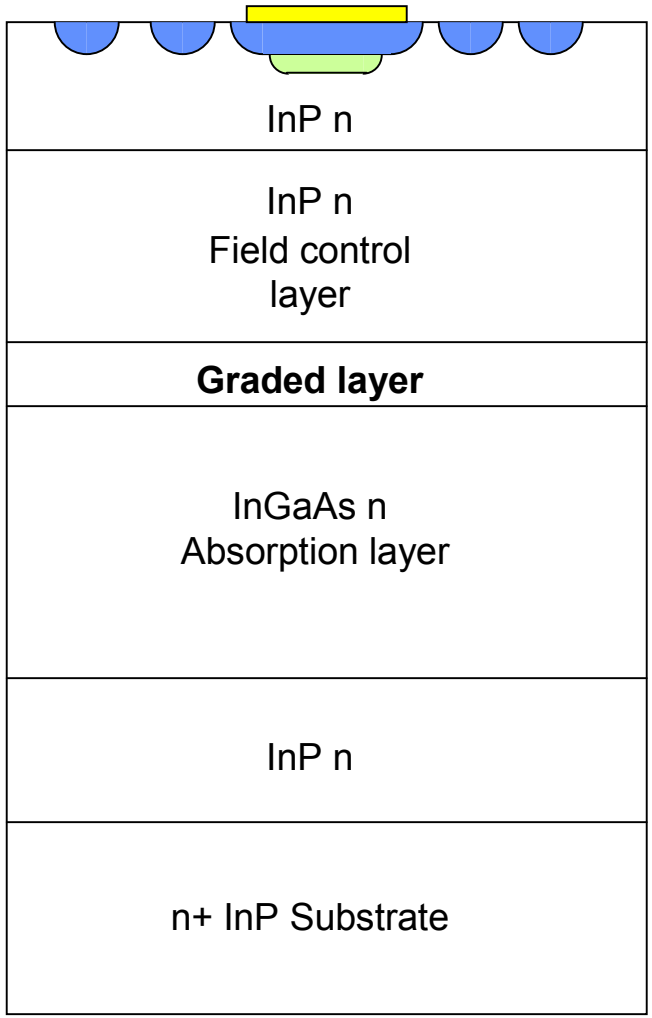
Φ=40μm p-i-n
9.7GHz bandwidth

InAlAs/InGaAs APD

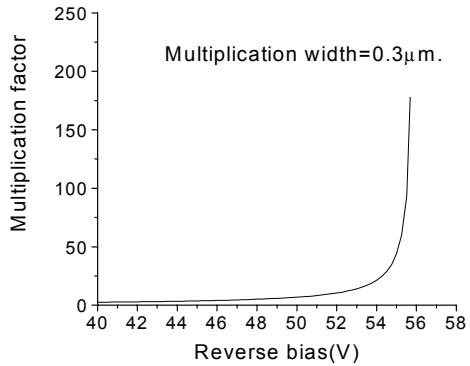


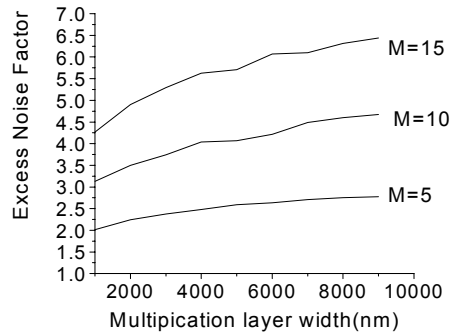


10Gbit APD with Floating Guarding Ring (FGR) Design

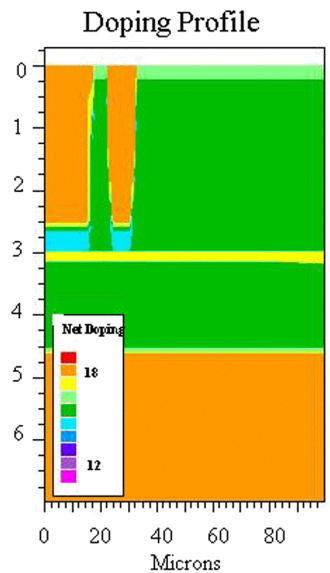


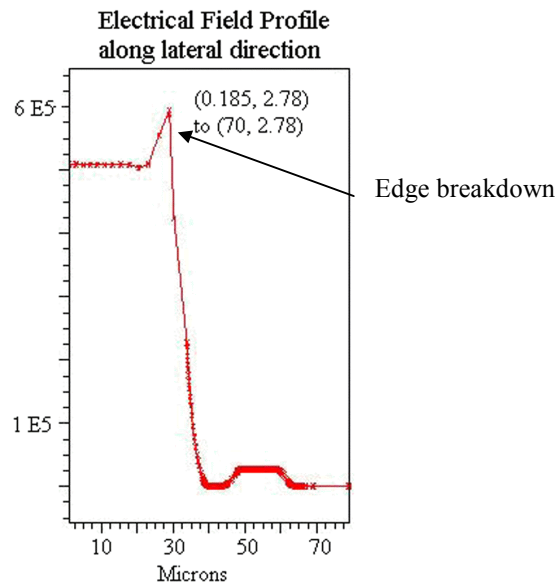
1D simulation



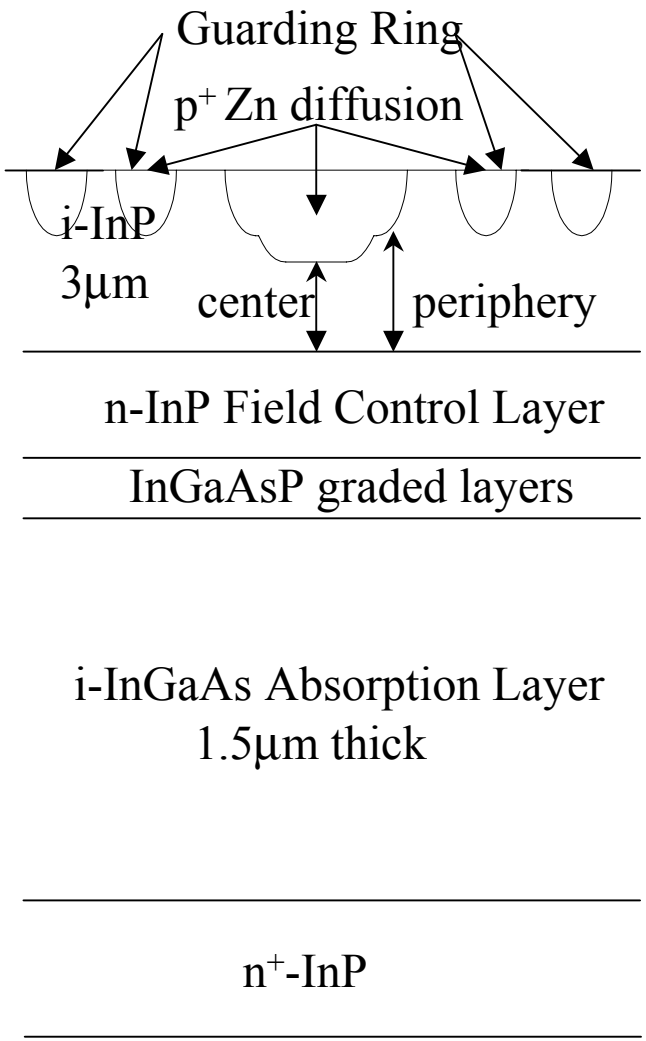


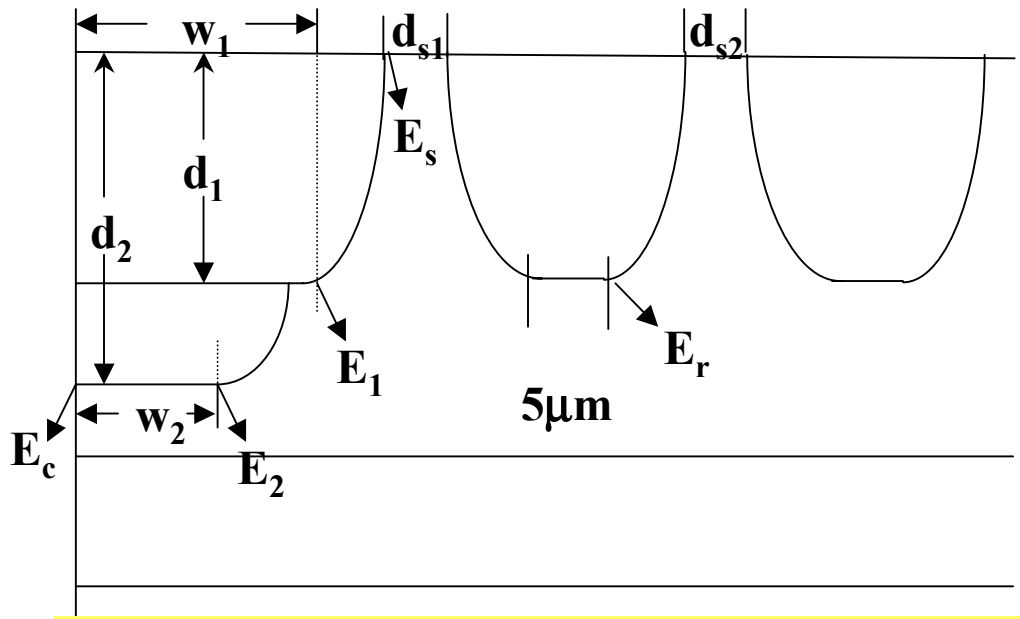
2D simulation





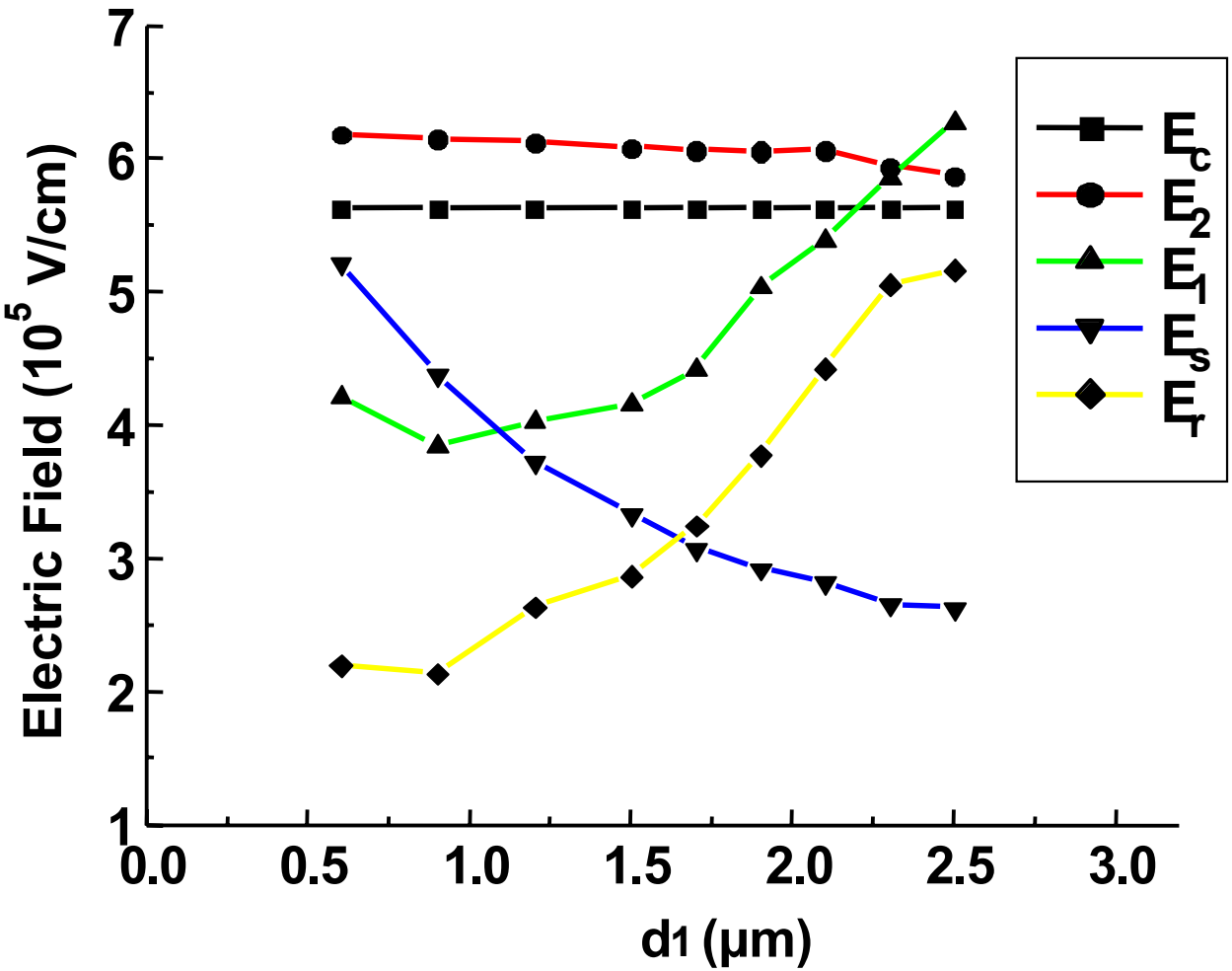
Double Diffused FGR Planar APD Structure and Design Parameters





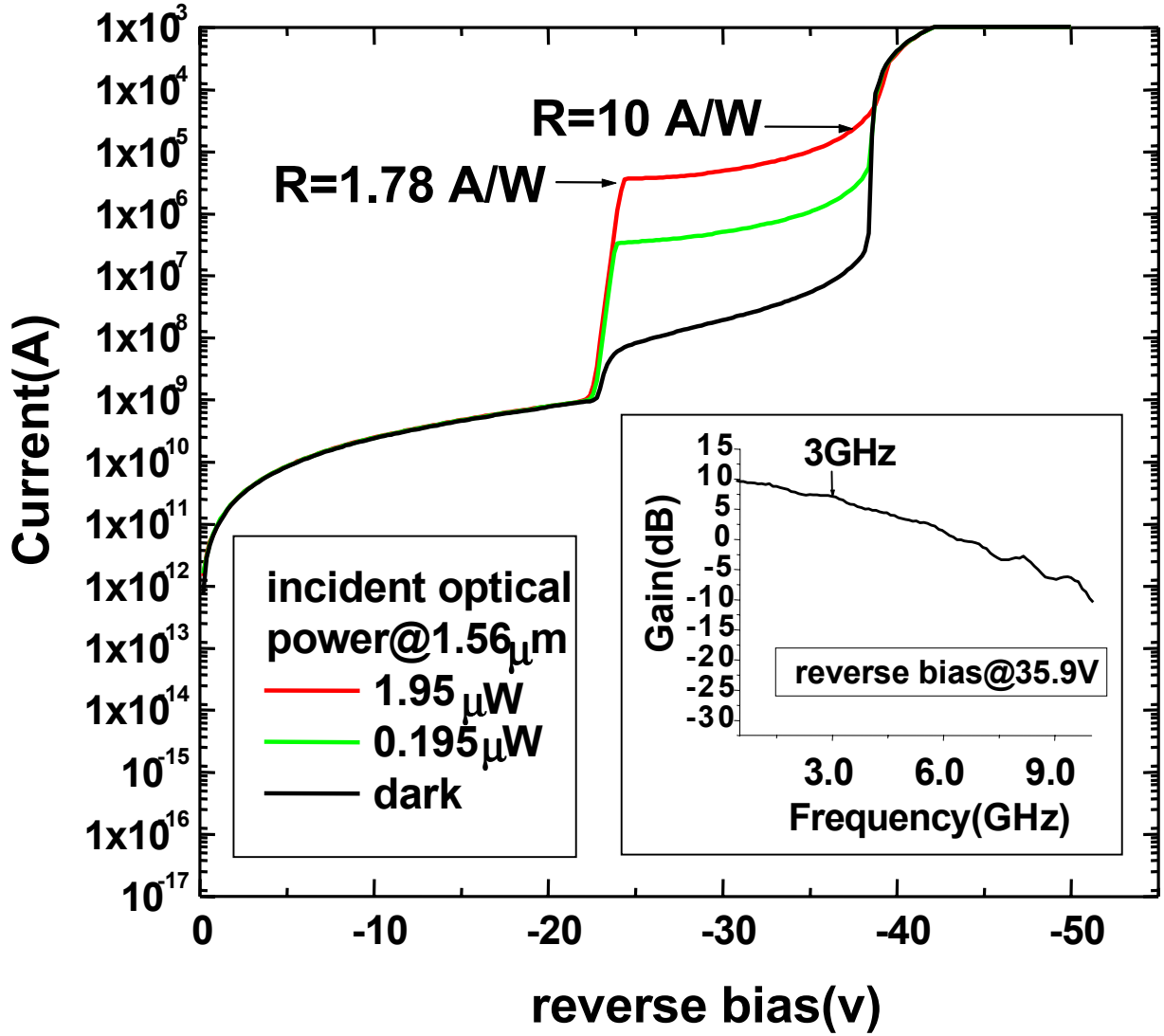
- Electric field in the multiplication layer must be > 4.5×10^7V/m for gain
- Electric field in the absorption layer must be < 2×10^7V/m to avoid tunneling and >1×10^7V/m for high bandwidth and efficiency
- Total charge in the field control layer should be 2.2-2.8 $\times10^{12}$ C·cm^{-2}

Design of Double Diffused FGR Planar APD



- Change of first diffusion depth.
- Other parameters are fixed at: $d_{s1}=d_{s2}=1.5\mu m$, $d_2=2.7\mu m$, $w_1=10\mu m$, $w_2=15\mu m$

Current-Voltage and Bandwidth Characteristics of FGR-APD



Progress and Future Milestones of APD Array Development Task

- Designed and fabricated an InAlAs/InGaAs APD/HEMT integrated receiver
- Fabricated low noise InAlAs ‘bulk’ and superlattice avalanche photodiodes with k=0.23
- Modeled floating guard ring APD for high yield, robust design for array applications
- Demonstrated 3GHz and 10GHz FGR APDs with high yield for arrays
- Future Work:
  - Integrate InAlAs into small array receivers

Summary

- Task I - VCSEL development
  - Demonstrate low-threshold InAlGaP injection lasers and VCSELs using native-oxide lateral carrier confinement near 670nm
  - Developed a robust wafer bonding process for long wavelength VCSEL fabrication
  - Demonstrated thermal and polarization stable photoluminescence in InGaAs quantum wires above 200Ksuitable for long wavelength VCSEL applications.
- Task II - Smart pixel array development
  - Direct extraction and accurate high frequency modeling of PIN photodetectors
  - InGaP/GaAs PIN/HBT 2x2 receiver array design and fabricated.
  - Designed 40 Gb/s HBT based single channel, bandwidth >34 GHz.
- Task III - Heterogeneous material integration
  - Demonstrated indium-based flip-chip bump bonding process
- Task IV - Avalanche photodiode array development
  - Fabricated high bandwidth (>10 GHz) InAlAs/InGaAs APD and InAlAs/InGaAs APD/HEMT receiver